PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte Furukawa et al.

Appeal No. _____

Appellants:	Furukawa et al.
Serial No.:	10/814,482
Filed:	March 31, 2004
Art Unit:	2818
Examiner:	David J. Goodwin
Title:	METHOD FOR FABRICATING STRAINED SILICON-ON-INSULATOR STRUCTURES AND STRAINED SILICON-ON-INSULATOR STRUCTURES FORMED THEREBY
Confirmation No.:	6082
Attorney Docket:	ROC920030399US1

Cincinnati, OH 45202 September 24, 2007

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

BRIEF ON APPEAL

I hereby certify that this correspondence for Application No. 10/814,482 is being electronically transmitted to Technology Center 2818, via EFS-WEB, on September 24, 2007.

/William R. Allen/
William R. Allen, Reg. No. 48,389

September 24, 2007
Date

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BRIEF ON APPEAL

I. Real Party in Interest

The real party in interest is International Business Machines Corporation of Armonk, New York, which is the assignee of the present invention.

II. Related Appeals and Interferences

There are no related appeals or interferences known to Appellants or Appellants' legal representative that will directly effect or be directly effected by or have a bearing on the decision of the Board in the present appeal.

III. Status of the Claims

Claims 1-15 stand rejected. Claims 1-15 are now on appeal.

IV. Status of Amendments

There have been no amendments filed subsequent to the final rejection dated July 11, 2007.

V. Summary of Claimed Subject Matter

Appellants' independent claim 1 is directed to a semiconductor structure. *See generally* Figs. 3 and 4; page 6, line 13 – page 9, line 6. The semiconductor structure comprises an island (18) of a semiconductor material, a handle wafer (14), and an insulating layer (16) disposed between the island (18) and the handle wafer (14). *See* Fig. 1; page 4, lines 20-23. The insulating layer (16) electrically isolates the island (18) of the semiconductor material from the handle wafer (14). *Id.* The island (18) includes a plurality of sidewalls (17, 19). *See* amended Figs. 2A and 3; amended paragraph beginning at page 6, line 1. The island also includes a strained region (32). See Figs. 3 and 4; page 6, line 13 – page 9, line 6. The insulating layer (16) contains a thickened region (visible in Figures 3 and 4 and coinciding with region (32)) underlying the strained region (32). *Id.* The thickened region transfers tensile stress to the strained region (32). *Id.*

VI. Grounds of Rejection to be Reviewed on Appeal

1. Claims 1-11 and 13-15 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Pub. No. 2003/0111699 to Wasshuber et al.

2. Claims 1-4, 6-12, 14, and 15 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Pub. No. 2004/0150042 to Yeo et al.

VII. Argument

Appellants respectfully submit that the Examiner's rejections of claims 1-15 are not supported on the record, and that the rejections should be reversed.

A. *Claims 1-11 and 13-15 were improperly rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Pub. No. 2003/0111699 to Wasshuber.*

The Examiner argues that claims 1-11 and 13-15 are anticipated under 35 U.S.C. § 102(e) by U.S. Pub. No. 2003/0111699 to Wasshuber (hereinafter *Wasshuber*). Anticipation of a claim under 35 U.S.C. § 102, however, requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros., Inc. v. Union Oil Co., 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), *quoted in* In re Robertson, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999). Absent express description, anticipation under inherency requires extrinsic evidence that makes it clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991), *quoted in* In re Robertson at 1951. "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Continental Can at 1749, *quoted in* In re Robertson at 1951.

Appellants respectfully submit that *Wasshuber* fails to anticipate claims 1-11 and 13-15 and, as such, the rejections thereof should be reversed. Appellants will hereinafter address the various claims that are the subject of the Examiner's rejection in order.

Independent Claim 1

Wasshuber fails to disclose "an island of a semiconductor material" and "an insulating layer disposed between said island and said handle wafer," as set forth in Appellants' claim 1. *Wasshuber* discloses an implanted region (512) formed by implanting "a desired species (e.g.,

such as carbon, germanium, oxygen, or the like)" into the semiconductor material of the substrate (514) to introduce tensile or compressive stress that is transferred to a channel region (524). *See* Paragraphs [0035], [0042]. However, *Wasshuber* fails to disclose that the implanted region (512) constitutes an insulating layer. In particular, *Wasshuber* fails to disclose that the semiconductor material in the implanted region (512) is modified by the implanted species such that the semiconductor material in region (512) is somehow transformed into an insulator.

Wasshuber discloses that region (12) is formed in the same manner as region (512). After the implantation, region (12) is described by *Wasshuber* as silicon that has experienced a volumetric expansion or contraction. *See* paragraph [0021]. *Wasshuber* does not describe that the region (12) of silicon is somehow transformed by the oxygen implantation into an oxide, but instead continues to refer to region (12) as being composed of silicon even after region (12) is implanted.

In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. *See* MPEP § 2131. Because *Wasshuber* fails to disclose "an insulating layer disposed between said island and said handle wafer," reversal of the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e) is therefore respectfully requested for this reason alone.

Claim 1 is patentable for additional reasons. Specifically, *Wasshuber* fails to disclose "said insulating layer containing a thickened region underlying said strained region," as set forth in Appellants' claim 1. In particular, *Wasshuber* fails to disclose that implanted region (512), which the Examiner alleges is an insulating layer and Appellants deny, has any portion that has a different thickness than any other portion. In particular, *Wasshuber* fails to disclose that any portion of the implanted region (512) expands or contracts by a different amount than any other portion of the region (512). For example, the region (512) shown in Figure 21 of *Wasshuber* has the same thickness across its entire width (i.e., the distance between the upper and lower edges of region (512) is independent of the location at which one evaluates the thickness of region (512)). It follows that region (512) has a uniform thickness. Consequently, even if region (512) is considered an insulating layer, which the Examiner alleges and Appellants dispute, its thickness is uniform. Region (512) is embedded in a substrate (514) of semiconductor material (e.g., silicon)

that is not implanted. Assuming that region (512) is silicon that is expanded relative to the surrounding substrate (514), then region (512) is arguably a thickened region of the semiconductor material of substrate (514). However, because region (512) has a uniform thickness and is embedded in a substrate (514) of semiconductor material (not an insulating material), region (512) cannot represent a thickened region of an insulating layer, as set forth in Appellants' claim 1.

In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. *See* MPEP § 2131. Because *Wasshuber* fails to disclose "said insulating layer containing a thickened region underlying said strained region," Appellants respectfully request reversal of the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e) for at least this additional reason.

Because *Wasshuber* fails to disclose "said insulating layer containing a thickened region underlying said strained region" it follows logically that *Wasshuber* also fails to disclose "said thickened region transferring tensile stress to said strained region," as also set forth in Appellants' claim 1. Instead, *Wasshuber* discloses that the implanted region (512) of the semiconductor substrate (514) is modified by expansion for transferring the tensile stress to the implanted region (512). A person having ordinary skill in the art would have understood that the semiconductor substrate (514), which is expanded by the implanted region (512) to transfer stress to the channel region (524), is not an insulating layer with a thickened region.

In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. *See* MPEP § 2131. Because *Wasshuber* fails to disclose "said thickened region transferring tensile stress to said strained region," Appellants respectfully request that the Board reverse the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e) for at least this additional reason.

Wasshuber also fails to disclose "said insulating layer electrically isolating said island of said semiconductor material from said handle wafer," as also set forth in Appellants' claim 1. Wasshuber fails to disclose that the channel region (524), which the Examiner has identified as the claimed "island," is electrically isolated from the substrate (514). Furthermore, Figure 22 of *Wasshuber* reasonably discloses and suggests to one of ordinary skill in the art that gaps

comprising semiconductor material of substrate (514) are disposed between the implanted region (512) and the isolation structures (535a, 535b). Consequently, *Wasshuber* does not disclose that the substrate (514) identified by the Examiner as the claimed "handle wafer" and channel region (524) identified by the Examiner as the claimed "island" are electrically isolated from each other, as expressly required by Appellants' claim 1. In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. *See* MPEP § 2131. Hence, reversal of the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e) is therefore respectfully requested for at least this additional reason.

By way of rebuttal, Appellants submit that the Examiner's remarks on pages 7 and 8 of the July 11, 2007 Office Action regarding the rejection over *Wasshuber* are clearly erroneous.

On page 7 of the July 11, 2007 Office Action, the Examiner contends that "when oxygen is implanted into silicon to form a buried layer, said buried layer will comprise silicon oxide by a means known to one of ordinary skill in the art as a chemical reaction." However, the Examiner has failed to appreciate that merely implanting oxygen into silicon does not in and of itself form oxide by a "chemical reaction." Oxide formed by implantation requires a highly specialized separation by implantation of oxygen (SIMOX) process, which *Wasshuber* fails to disclose. A SIMOX process requires an extremely high implanted dose of oxygen that exceeds the solid solubility limit of oxygen in silicon and then a thermal anneal to transform the implanted zone into an oxide layer. *Wasshuber* also fails to disclose that the implanted oxygen forms an oxide layer or any other type of layer with electrically insulating properties, and fails to disclose that region (512) is an insulator. This strengthens Appellants' rebuttal argument that the mere disclosure of the implantation of oxygen in *Wasshuber* does not necessarily result in the formation of an insulating layer by a "chemical reaction" as contended by the Examiner. Additional steps of a highly specialized nature must be taken to promote a chemical reaction between oxygen and silicon sufficient to define an insulating layer from a "buried layer"; none of which are disclosed in *Wasshuber*. Hence, the Examiner's rebuttal argument is not technically sound.

On page 7 of the July 11, 2007 Office Action, the Examiner further contends that "Wasshuber explicitly states that the buried layer comprises a volumetric expansion (paragraph 0035)" and that "when a layer undergoes a volumetric expansion it 'thickens'." However, the Examiner fails to appreciate that the thickened layer allegedly disclosed as region (512) in *Wasshuber* is not a thickened insulating layer, but instead arguably represents a thickened region of silicon. Even if region (512) were considered to be the insulating layer, which the Appellants deny, its thickness is uniform across its entire width and, consequently, no portion of region (512) is thicker than any other portion of region (512). Hence, the Examiner's rebuttal argument is not technically sound.

In the context of Appellants' argument that "Wasshuber does not teach that any part of the buried layer undergoes more thickeneing *(sic)* than any other part of said layer," the Examiner contends on pages 7 and 8 of the July 11, 2007 Office Action that "the features upon which applicant relies (i.e., a thickening differential) are not recited in the rejected claims." However, the Examiner fails to appreciate that the "thickening differential" is *de facto* set forth in claim 1 as the recited "thickened region." Specifically, claim 1 recites "said insulating layer containing a thickened region underlying said strained region" of the island of semiconductor material.

On page 8 of the July 11, 2007 Office Action, the Examiner further contends that "in figure 20, electrically isolating trenches (531a,b) and electrically isolating buried oxide (512). A person having ordinary skill in the art would understand that a semiconducting island surrounded by electrically isolating structures is an electrically isolated semiconducting island." However, the Examiner fails to appreciate the trenches (531a,b) in *Wasshuber* electrically isolate the island of semiconductor material from adjacent islands, not from the underlying substrate. The Examiner also fails to appreciate that the object labeled with reference numeral (512) in *Wasshuber* is not a "buried oxide." Instead, the object labeled with reference numeral (512) in *Wasshuber* is an implanted region (512) and is not an oxide for reasons set forth hereinabove. Hence, the Examiner's rebuttal argument is not technically sound.

Dependent Claims 2-11 and 13-15

Claims 2-11 and 13-15 are not argued separately.

B. *Claims 1-4, 6-12, 14, and 15 were improperly rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Pub. No. 2004/0500429 to Yeo et al.*

The Examiner argues that claims 1-4, 6-12, 14, and 15 are anticipated under 35 U.S.C. § 102(e) by U.S. Pub. No. 2004/0150042 to Yeo et al. (hereinafter *Yeo*). Anticipation of a claim under 35 U.S.C. § 102, however, requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros., Inc. v. Union Oil Co., 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), *quoted in* In re Robertson, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999). Absent express description, anticipation under inherency requires extrinsic evidence that makes it clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991), *quoted in* In re Robertson at 1951. "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Continental Can at 1749, *quoted in* In re Robertson at 1951.

Appellants respectfully submit that *Yeo* fails to anticipate claims 1-4, 6-12, 14, and 15 and, as such, the rejections thereof should be reversed. Appellants will hereinafter address the various claims that are the subject of the Examiner's rejection in order.

Independent Claim 1

Yeo fails to disclose "said insulating layer containing a thickened region underlying said strained region," as set forth in Appellants' claim 1. In particular, *Yeo* fails to disclose that the insulating layer (54) identified by the Examiner has any portion with a different thickness than any other portion. Hence, it follows logically that *Yeo* fails to disclose a thickened region in insulating layer (54). In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. *See* MPEP § 2131. Because *Yeo* fails to disclose "said insulating layer containing a thickened region underlying said

strained region," *Yeo* fails to anticipate claim 1. Hence, Appellants respectfully request that the Board reverse the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e) for at least this reason.

Claim 1 is patentable for additional reasons. Because *Yeo* fails to disclose "said insulating layer containing a thickened region underlying said strained region," it follows that *Yeo* fails to disclose "said thickened region transferring tensile stress to said strained region," as also set forth in Appellants' claim 1. Instead, *Yeo* merely discloses that a strained silicon layer (56) is provided on the insulating layer (54). *Yeo* does not disclose that the insulating layer (54) transfers stress in any manner or by any mechanism to the strained silicon layer (56).

In fact, *Yeo* discloses in Paragraph [0031] that:

> The thickness of the strained silicon layer ranges from 10 angstroms to 500 angstroms which may be formed by a layer transfer technique. An example of a layer transfer technique is a wafer bonding step followed by a wafer separation step. In the wafer bonding step, a donor wafer comprising a strained silicon layer overlying a relaxed silicon-germanium layer is bonded to a target wafer comprising a silicon oxide layer overlying a silicon substrate, such that the strained silicon layer is in atomic contact with the silicon oxide layer. In the subsequent wafer separation step, the strained silicon layer is separated from the donor wafer so that a new final wafer is formed comprising a strained silicon layer overlying a silicon oxide layer which is (*sic*) turn overlies a silicon substrate.

Based on this reproduced passage from *Yeo*, the silicon layer (56) is strained before layer (56) is bonded by a "layer transfer technique" to the insulating layer (54) of "silicon oxide" on a "target wafer." Specifically, *Yeo* discloses in paragraph [0031] that the silicon layer (56) is strained when the silicon layer (56) deposited on a "relaxed silicon-germanium layer" that is itself on a "donor wafer," which occurs in the processing sequence before the silicon layer (56) is bonded to the insulating layer (54).

In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. *See* MPEP § 2131. Because *Yeo* fails to disclose "said thickened region transferring tensile stress to said strained region," Appellants respectfully request that the Board reverse the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e) for at least this additional reason.

Dependent Claims 2-4, 6-12, 14, and 15

Claims 2-4, 6-12, 14, and 15 are not argued separately.

VIII. Conclusion

In conclusion, Appellants respectfully request that the Board reverse the Examiner's rejections of claims 1-15 and that the application be passed to issue. If there are any questions regarding the foregoing, please contact the undersigned. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account No. 23-3000.

Respectfully submitted,
WOOD, HERRON & EVANS, L.L.P.

Date: September 24, 2007

By: /William R. Allen/
William R. Allen, Reg. No. 48,389

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APPENDIX OF CLAIMS

1. (Previously Presented) A semiconductor structure comprising:

an island of a semiconductor material, said island including a plurality of sidewalls and a strained region;

a handle wafer; and

an insulating layer disposed between said island and said handle wafer, said insulating layer containing a thickened region underlying said strained region, said insulating layer electrically isolating said island of said semiconductor material from said handle wafer, and said thickened region transferring tensile stress to said strained region.

2. (Previously Presented) The semiconductor structure of claim 1 wherein said insulating layer is a buried oxide layer and said island is silicon.

3. (Previously Presented) The semiconductor structure of claim 1 further comprising:

a source defined in said island;

a drain defined in said island; and

a channel defined in a portion of said island between said source and said drain, said channel disposed at least partially in said strained region of said island.

4. (Previously Presented) The semiconductor structure of claim 3 further comprising:

a gate electrode electrically isolated from said portion of said island defining said channel.

5. (Original) The semiconductor structure of claim 4 wherein said strained region divides said gate electrode.

6. (Original) The semiconductor structure of claim 4 wherein said gate electrode generally overlies said channel.

7. (Previously Presented) The semiconductor structure of claim 1 further comprising:

a semiconductor device fabricated using said island.

8. (Previously Presented) The semiconductor structure of claim 1 wherein said island is silicon and said thickened region of said insulating layer is formed by oxidation of said island.

9. (Original) The semiconductor structure of claim 9 wherein said insulating layer is silicon dioxide.

10. (Previously Presented) The semiconductor structure of claim 9 wherein said handle wafer is silicon and said thickened region is formed by oxidation of said handle wafer.

11. (Original) The semiconductor structure of claim 1 wherein said tensile stress is effective to enhance carrier mobility within said strained region.

12. (Original) The semiconductor structure of claim 1 wherein a thickness of said thickened region is increased by an increment in the range of about 5 nanometers to about 10 nanometers.

13. (Original) The semiconductor structure of claim 1 wherein said thickened region of said insulating layer has a thickness greater than that of surrounding regions of said insulating layer flanking said thickened region.

14. (Previously Presented) The semiconductor structure of claim 1 further comprising:

first and second anchors flanking said strained region, said first and second anchors effective for limiting relaxation of said strained region of said island.

15. (Previously Presented) The semiconductor structure of claim 14 wherein said first and second anchors comprise adjacent regions of said island flanking said strained region.

16-34. (Cancelled)

APPENDIX OF EVIDENCE

(None)

APPENDIX OF RELATED PROCEEDINGS

(None)